Six Bit Digital Phase Shifter using Lumped Network for ST Radar

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ABSTRACT

In electronically scanned antenna array, the antenna beam-steering in the desired direction without physically repositioning the antenna can be made possible by use of phase shifters, which can be implemented in the transmit receive path of the antenna. For Stratospheric Tropospheric (ST) Radar, the six bit digital phase shifter using lumped components equivalent of transmission line has been designed and implemented. This phase shifter is designed in order to achieve proper beam-positioning, 360° azimuthal angle and ±15° elevation angle. This phase shifter is a part of transmit-receive (TR) module which is associated with each antenna in the circular array of 576 Yagi-Uda antennas. The results of this design are obtained in terms of insertion loss, return loss, phase error and verified computationally using Matlab and simulations in ADS (Advanced Design System) software. The six bit digital phase shifter has been fabricated using FR4 substrate and the results are measured in Vector Network Analyzer (VNA) for all possible combinations of phase shifts at 212MHz frequency.

General Terms

Phased Array Antennas, Transmit Receive (TR) Module

Keywords

Phase Shifter, ST Radar, Lumped Networks

1. INTRODUCTION

Phase shifters are classified as two port networks. Phase shifter modifies the phase of the input signal and gives the modified output signal. Amount of change in phase may be controlled by having a control logic circuit, digital control circuit or analog dc bias control circuit, accordingly these can be classified as digital or analog phase shifters respectively. Digital phase shifter which shows only predetermined changes in discrete steps, for e.g. 180°, 90°, 45° ...11.25° have found extensive applications in designing phased array antenna system, frequency up-converters and phase modulators [1]. There are several methods to realize digital phase shifter which include switched-network phase shifter where change in the output phase is obtained by varying switching frequency between two phase shifter networks and it results into a desired differential phase shift. Such networks can be implemented using the combination of low-pass filter and high-pass filter or they can be sections of transmission lines of different lengths which behave as phase shifter [1], [4], [9], [8], [2]. Other method to realize phase shifters is the transmission-line type method where a piece of transmission line results into the desired phase shift [5], [10], [3].

The work presented here focuses on the development of digital phase shifter for Stratospheric Tropospheric Radar (ST Radar). This phase shifter has six bit control logic to control the phase shift. It is a high resolution Radar system, which uniquely provides the critical atmospheric parameters of vertical component of wind flow to investigate Stratosphere and Troposphere (ST) layer of atmosphere. It has been designed and developed by Society for Applied Microwave Electronics Engineering and Research (SAMEER), Department of Electronics and Information Technology (DeitY) Powai, Mumbai for the Gauhati University, Aasam. The realization of this ST Radar is done using circular array of 576 Yagi Uda antennas, with the beam-steering capability, azimuthal angle of 360° with ±15° elevation angle. In order to achieve this beam-positioning each antenna has its own Transmit-Receive (TR) Module which consists of digital phase shifter. This phase shifter is instrumental in adjusting the phase of RF Signal which is fed to the corresponding antenna as per the Radar controller data. To design this phase shifter, earlier the former approach of switched network type phase shifter was adapted and from the literature [1], it was mathematically found that, transmission phase at the desired operating frequency of 212 MHz was quite large. After that the transmission line approach to obtain the required phase shift was analyzed in order to implement these differential phase shifts and it was found that 35.35 cm of transmission line is required to obtain phase shift of 90 degree at 212MHz, which is large enough and would considerably increase the size of the complete design [7].

The key contribution presented here is the design and implementation of the 6-bit digital phase shifter using the Lumped element, equivalent of the Transmission line. Block diagram of the phase shifter has been discussed in Section 2, followed by the mathematical design in Section 3. This design has been verified computationally in Matlab and further simulated using ADS (Advanced Design System) software. Results are presented in Sections 4 and 5. After computational verification, schematic as developed for the entire design and is subsequently explained in Section 6. Actual implemented design along with the comparison of measured and computed results is concluded in Section 7.

2. PHASE SHIFTER BUILDING BLOCKS

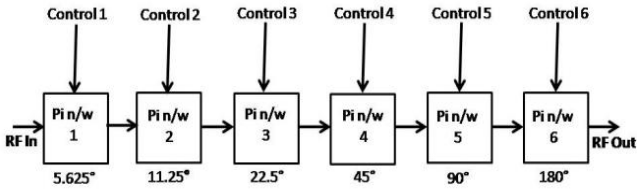

Fig.1. Block diagram of six bit digital phase shifter

Block diagram of the phase shifter designed is shown in Fig. 1. It consists of six different blocks each corresponds to a change of $1 - bit$ in order to introduce phase shifts with a resolution of 5.625°. In particular, individual blocks are designed that results to the phase shifts of 5.625°, 11.25°, 22.5°, 45°, 90° and 180°. These blocks are arranged in cascade and are controlled by six bit digital control logic. The desired phase shift/ beam angle is provided to the TR module by the radar controller. Accordingly the TR module controller generates a control signal for the digital phase shifter to acquire the desired phase shift. Since the control signal is digital in nature, the complete system results into 64 combinations of phase states with the discrete change of 5.625° between any two successive states. Each basic building block is implemented as a lumped network, output of which provides a required phase change in the input RF signal. This lumped network is equivalent to a piece of transmission line which would have provided the required phase shift. Each successive block corresponds to a phase shift of 5.625, 11.25, 22.5, 45, 90 and 180 degree respectively.

3. MATHEMATICAL DESIGN OF PHASE SHIFTER

We present a synthesis for a piece of transmission line of length l using lumped network in order to provide a required phase shift. From literature [6], at the operating frequency of 212 MHz the size of the lumped elements is not comparable to the wavelength. Thus the distributed parameters of transmission line do not dominate the performance. The transmission line has been assumed to be equivalent to a basic ∏ network, Tee network, L network or any other network. Thus by properly synthesizing the circuit element values, the desired phase shift has been obtained. The derivation for equivalent lumped components considering the modeling of transmission line as a ∏ network has been presented (refer Fig.2).

Fig.2. ∏ network equivalent for a transmission line

Let, βl be the length of transmission line in radians and Z_o be its characteristic impedance. Let Y and Z be the admittance and impedance of the equivalent lumped elements, respectively. As per the cascading property of ABCD parameters we write the cascaded ABCD parameters of the lumped network to be equal to the transmission line parameters.

$$\begin{bmatrix}1 & 0\\ Y & 1\end{bmatrix}\begin{bmatrix}1 & Z\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ Y & 1\end{bmatrix} = \begin{bmatrix}cos\beta l & jZ_o sin\beta l\\ jsin\beta l/Z_o & cos\beta l\end{bmatrix}$$

which can be simplified as

$$\begin{bmatrix}1+YZ & Z\\ Y(2+YZ) & 1+YZ\end{bmatrix} = \begin{bmatrix}cos\beta l & jZ_o sin\beta l\\ jsin\beta l/Z_o & cos\beta l\end{bmatrix}$$

Considering the series element to be an inductor and shunt elements to be capacitors, we get

$$\begin{bmatrix}1+j^2\omega^2 LC & j\omega l\\ j\omega C(2+j^2\omega^2 LC) & 1+j^2\omega^2 LC\end{bmatrix} = \begin{bmatrix}cos\beta l & jZ_o sin\beta l\\ jsin\beta l/Z_o & cos\beta l\end{bmatrix}$$

This implies to the following equation which can be used for computing the actual values of the inductor and capacitors in lumped network.

$$1 + j^2\omega^2 LC = cos\beta l$$

$$j\omega l = jZ_o sin\beta l \qquad (1)$$

We now present the reverse synthesis for the ∏ network to compute the S parameters which has been further verified computationally using MATLAB and presented in section 5.

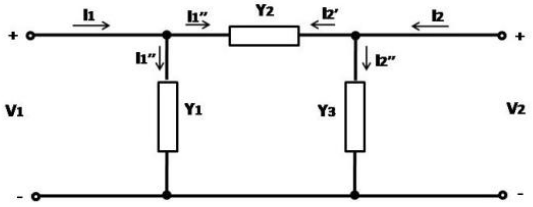

Fig. 3. ∏ network

Form Fig. 3, we derive,

$$I_1 = (Y_1 + Y_2)V_1 - Y_2 V_2$$

$$I_2 = -Y_2 V_1 + (Y_1 + Y_3)V_2$$

$$Y = \begin{bmatrix}(Y_1+Y_2) & -Y_2\\ -Y_2 & (Y_1+Y_3)\end{bmatrix} \qquad (2)$$

Considering the Y_1 and Y_3 as shunt capacitors and Y_2 as series inductor,

$$Y_1 = Y_3 = \frac{j}{\omega C}$$

and,

$$Y_2 = \frac{1}{j\omega L}$$

Hence the admittance matrix elements in terms of lumped network parameters can be expressed as,

$$Y_{11} = Y_{21} = \frac{1-\omega L}{j\omega^2 LC}$$

$$Y_{12} = Y_{21} = \frac{1}{\omega L}$$

$$Y = \begin{bmatrix} (\frac{1-\omega l}{j\omega^2 LC}) & (\frac{1}{\omega L}) \\ (\frac{1}{\omega L}) & (\frac{1-\omega L}{j\omega^2 LC}) \end{bmatrix}$$

This Y matrix can be obtained for each lumped network and can be converted into its respective $ABCD$ network by using $A = \frac{-Y_{22}}{Y_{21}}$, $B = \frac{-1}{Y_{21}}$, $C = \frac{-|Y|}{Y_{21}}$, $D = \frac{-Y_{11}}{Y_{21}}$, where $|Y| = Y_{11} * Y_{22} - Y_{12} * Y_{21}$ and $\Delta Y = (Y_{11} + Y_o)(Y_{22} + Y_o)$ [6]. These $ABCD$ parameters can thus be calculated for all the network and due to its cascading property the $ABCD$ matrix for the entire circuit can be obtained. Similarly the desired S Parameters are obtained according to the input control signal which in turn verifies the results for the specific values of inductor and capacitors.

The S parameters for each network can also be obtained directly from its Y parameters by;

$$S_{11} = \frac{(Y_o + Y_{11})(Y_o + Y_{22} + Y_{12}Y_{21})}{\Delta Y}$$

$$S_{21} = \frac{-2Y_{21}Y_o}{\Delta Y}$$

After simplifying, we get S_{11} and S_{21} in terms of L and C as mentioned in (4) and (5).

$$S_{11} = \frac{[Y_o + \frac{1-\omega L}{j\omega^2 LC}]^2 + [\frac{1}{\omega L}]^2}{[Y_o + \frac{1-\omega L}{j\omega^2 LC}]^2 - [\frac{1}{\omega L}]^2}$$

$$S_{21} = \frac{2\omega LCY_o}{C(1+\omega^2 L^2 Y_o) + jL(1-\omega)}$$

We now present an example for the phase shift of 45°, which results in $\beta l = 0.78539$ rad, to calculate the lumped elements for the equivalent $\prod$ realization using (1).

$$L = \frac{Z_o sin\beta l}{\omega}$$

$$C = \frac{1-(cos\beta l)}{\omega L^2}$$

Hence the required values for this network to provide the desired phase shift of 45° are $L = 26.54$ nH and $C = 6.21$ pF. The calculated values of $Y, ABCD, S$ parameters are

$$[Y] = \begin{bmatrix} 0 - 0.0200j & 0.0283 \\ 0 + 0.023 & 0 - 0.0200 \end{bmatrix}$$

$$[ABCD] = \begin{bmatrix} 0.7071 & 0 + 35.3562 \\ 0 + 1.141j & 0.7071 \end{bmatrix}$$

$$[S] = \begin{bmatrix} 0.0000 + 0.0000j & 0.7071 - 0.7071j \\ 0.7071 - 0.7071j & 0.0000 + 0.0000j \end{bmatrix}$$

By using these calculated values of lumped elements we obtain the phase shift of -44.996° and insertion loss of -2.1770x10^{-9} dB.

$$Magnitude\ S_{21}(rad) = 1.000$$
$$Magnitude\ S_{21}(dB) = -2.1770x10^{-9}$$
$$Phase\ S_{21}(rad) = -0.7854$$
$$Phase\ S_{21}(degree) = -44.9996$$
$$Magnitude\ S_{11}(rad) = 2.2389x10^{-5}$$
$$Magnitude\ S_{11}(rad) = -92.9992$$

These mathematical calculations are further verified in ADS and results are shown in Fig. 4 and Fig.5

4. SIMULATION RESULTS

The values for L and C obtained from the mathematical calculation were used to verify the circuit design using ADS simulation tool. Fig. 4 shows the design implementation for lumped network to result in phase shift of 45 degree in ADS and the results of this design are depicted in Fig.5.

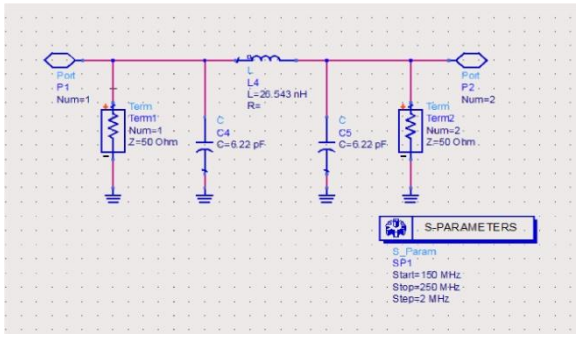

Fig.4. Design for 45 degree phase shift in ADS

It is seen that the phase shift (phase of S_{21}) achieved is -45.003 degree with the insertion loss (magnitude of S_{21}) and return loss (magnitude of S_{11}) of -2.65E-9 dB and -92.145dB, respectively. Fig.6 shows the design implementation for 4 cascaded lumped network blocks to result in phase shift of 175.375 degree using ADS and Fig.7 depicts the corresponding results.

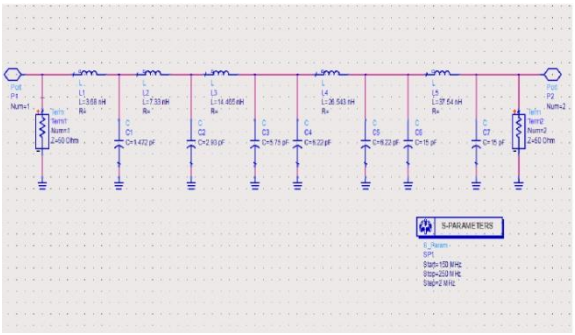

Fig.6. Design for 175.375 degree phase shift in ADS

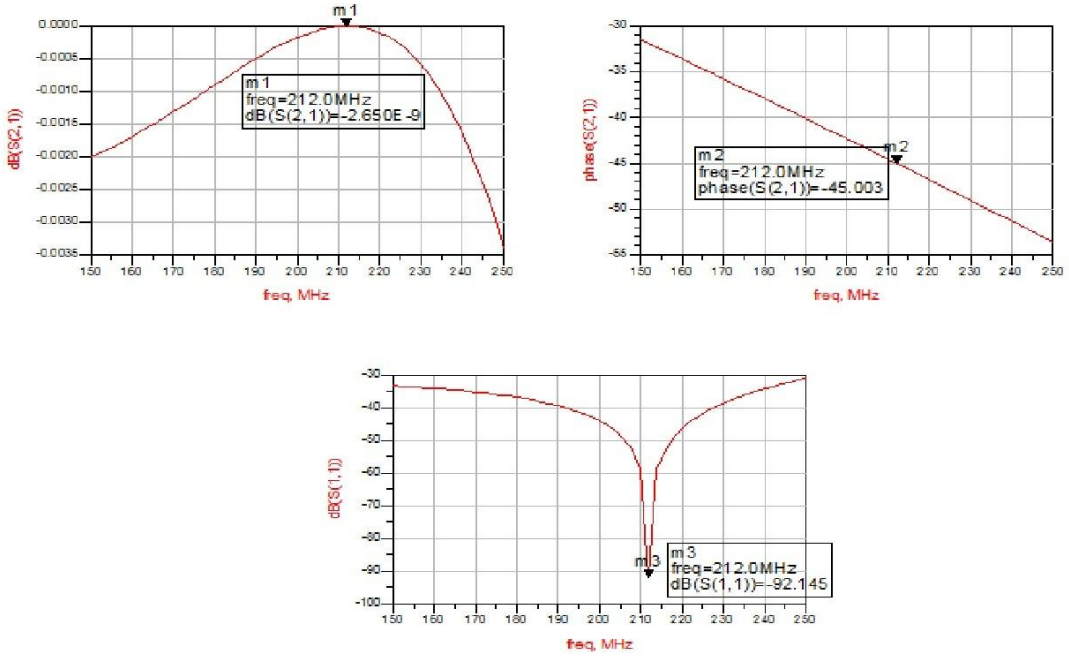

Fig. 5. Simulation Result for 45 degree phase shift

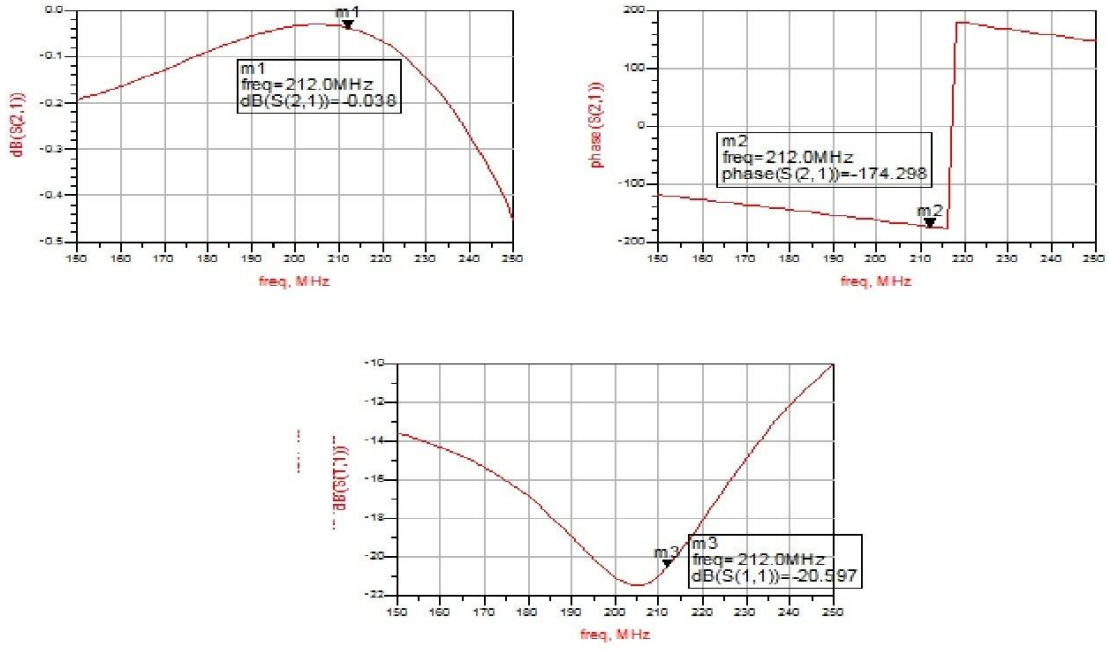

Fig.7. Simulation Result for 175.375 degree of phase shift

5. COMPUTATIONAL RESULTS

In Fig. 8 and Fig. 9, we present insertion loss and return loss, respectively, by varying frequency. Specifically, we compute the maximum, Root Mean Square (RMS), minimum and Standard deviation values of insertion loss and return loss for different frequencies. As depicted, the insertion loss is close to 0 dB for most of the frequencies along with the desired frequency range. Further, the maximum return loss has been observed to be less than -15dB for the entire frequency range as seen in figure 9. All the computations were carried out using MATLAB. The phase error have been computed for a range of frequencies with the designed circuit. The Worst case error, absolute mean and the RMS error plots are shown in the Fig.10. Fig.11 and Fig.12 presents the computed insertion and return loss, respectively, for various frequencies. The different curves in the figure represents plots for all possible 64 phase states. These values indicate the desired performance at 212MHz of frequency for which the circuit has been designed. As seen, the return loss attains minimum value at 212MHz which in turn implies the maximum matching at the design frequency.

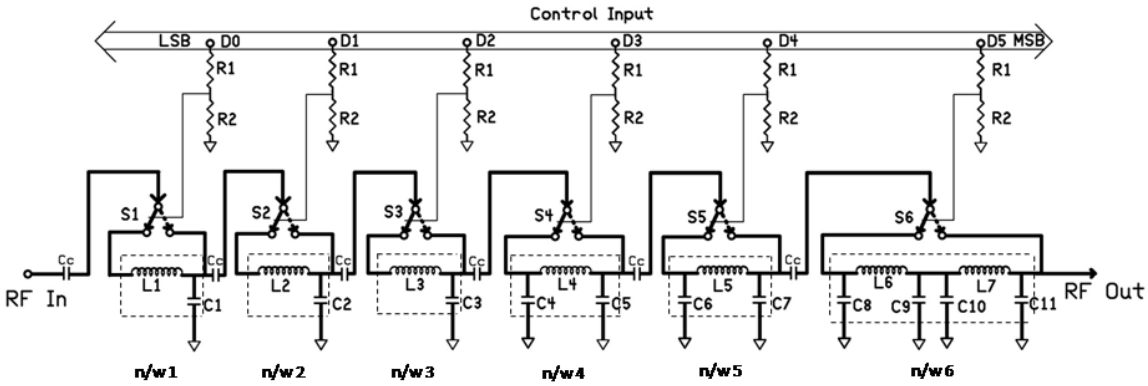

Fig.13. Schematic of the six bit digital phase shifter

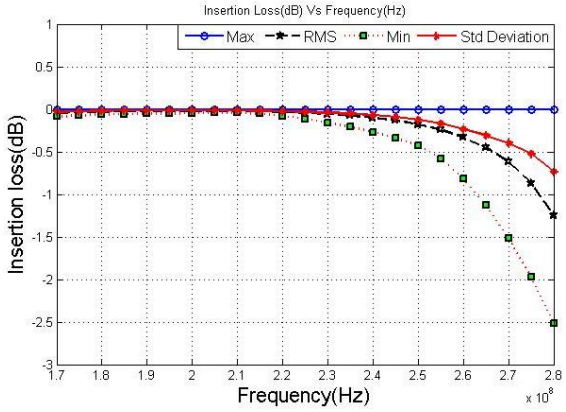

Fig. 8. Insertion loss with respect to frequency considering all 64 phase states

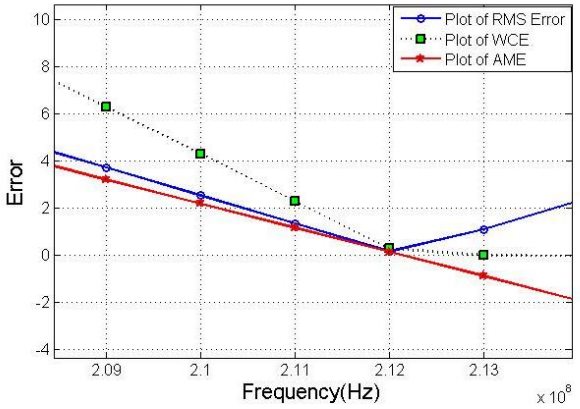

Fig. 10. Phase Error with respect to frequency considering all 64 phase states

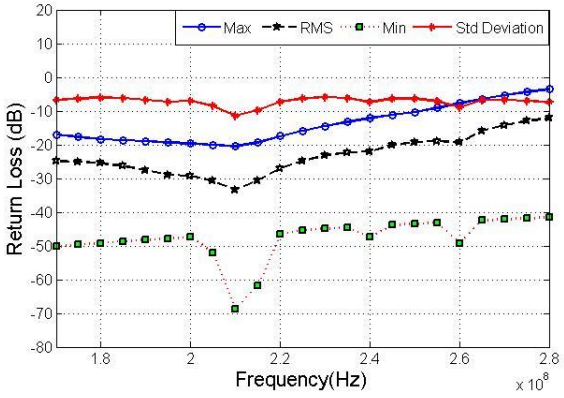

Fig. 9. Return loss with respect to frequency considering all 64 phase states.

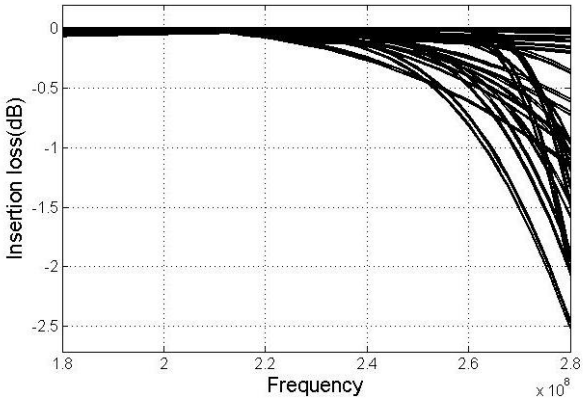

Fig. 11. Design Performance in terms of Insertion loss with respect to frequency for various phase shifts for circuit designed at frequency of 212MHz

6. IMPLEMENTATION OF SIX BIT DIGITAL PHASE SHIFTER

Fig. 13 presents the Schematic diagram of the six bit digital phase shifter. Six different lumped networks have been designed and arranged in cascade. The values of lumped elements to result in desired phase shifts are calculated mathematically, and used in actual design. Two port L and ∏ networks has been adapted for designing of all the blocks. The L network provide the corresponding phase shifts of 5.625, 11.25 and 22.5 degrees and the design for blocks enabling phase shift of 45 and 90 is two port ∏ network. The phase shift of 180 degree is implemented by cascading two ∏ network each having a phase shift of 90 degrees. All these lumped network blocks are controlled with the help of dual SPDT switches which are implemented between the two successive L/∏ networks for selection of the particular network. Whenever the control input bit to a particular network block is high, phase of RF signal passing through that

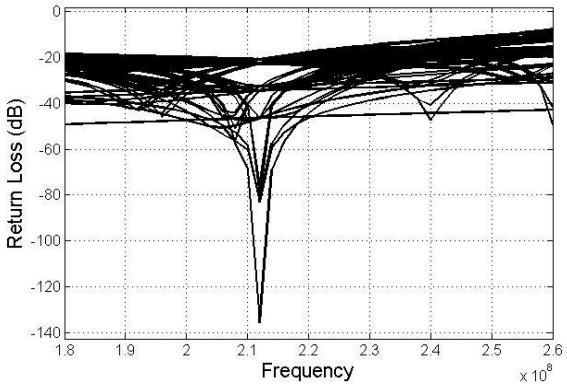

Fig. 12. Design Performance in terms of Return loss with respect to frequency for various phase shifts for circuit designed at frequency of 212MHz

corresponding network gets modified and adds to the overall phase shift. In case of low control input bit the L/∏ network is bypassed. These switches are connected in series to enhance the isolation between the input and the output of the RF signal. Coupling capacitors have been used between the two successive networks to block the dc component in the RF path. As these networks have the basic filtering property, the overall phase shifter design acts as perfectly matched at the operating frequency of 212 MHz and is clearly seen from the MATLAB result in Fig. 12. In this paper, six bit digital phase shifter has been designed using the lumped equivalent network of transmission line. A basic L network, _ network, tee network serve as the basic building blocks and are approximated to a unit length of a transmission line.

7. MEASURED RESULTS

The six bit digital phase shifter has been practically implemented and fabricated using the FR4 glass epoxy substrate of 1.59mm thickness with the copper clad of 0.036 mm, having the dielectric constant of 4.4. This phase shifter PCB has been populated by using the inductors and capacitors, the values of which are calculated from the above mathematical expressions [refer Section 3]. In this section, we discuss the measured results obtained from the implemented circuit. The measurements were carried out using Vector Network Analyzer for the losses and phase variation with the change in the 6 bit digital control input. The image of the layout design is shown in Fig. 14 and the implemented circuit has been shown in Fig. 15.

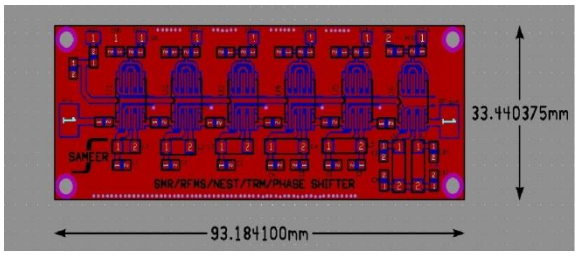

Fig. 14. PCB layout of the circuit diagram

In Fig. 16, the plot of phase error for designed six bit digital phase shifter obtained practically and computationally has been depicted. It can been seen that measured error is significantly less than the half bit error for six bit digital phase shifter.

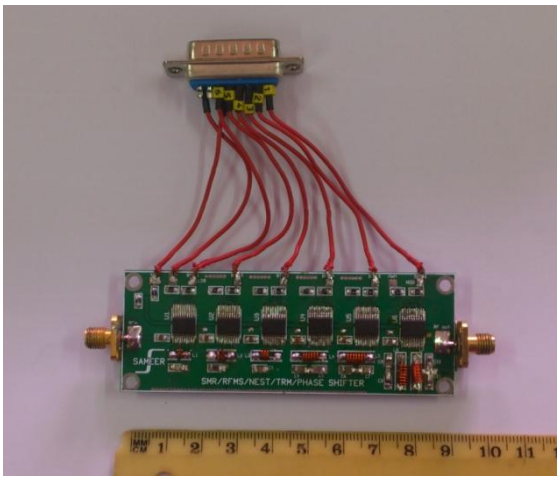

Fig.15. Fabricated circuit design

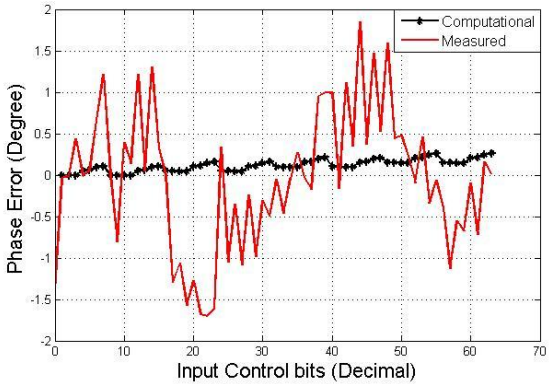

Fig.16. Measured and Computed Error with respect to 64 Digital Control Input Bits

In Fig. 17, we present the results obtained for insertion loss and return loss from the implemented circuit and compare these with the mathematically computed results. Almost constant insertion loss of -6 dB is observed in the implemented circuit. We also observe the comparable performance for the return loss.

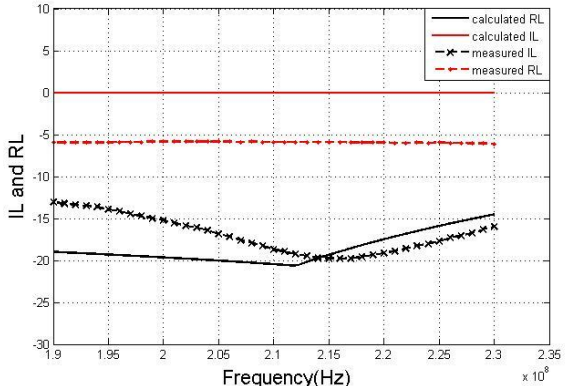

Fig. 17. Insertion loss and Return loss

8. CONCLUSION

Six bit digital phase shifter has been successfully designed and implemented. This design has been proposed for the Transmit Receive Module of 576 circular array antenna in Stratospheric Tropospheric (ST) Radar project. The logical design to result into the desired output signal depending on the input control bits has been developed, which was further supported with mathematical modeling. After mathematically obtaining the desired lumped element values, the design was verified using Advanced Design System (ADS) simulation tool and also verified computationally in MATLAB. The phase shifter has been practically implemented and tested in Vector Network Analyzer (VNA). The design was fabricated using FR4 glass epoxy substrate of 1.59mm thickness with the copper clad of 0.036 mm and having the dielectric constant of 4.4. The designed system has been realized with PCB 93.18 x 33.44 mm^2 in size. The results from the implemented PCB show the comparable performance to that of computed results. This phase shifter has been tested for all the 64 combinations of phase states and it resulted in the insertion loss of 5.8±0.4 dB and return loss of less than -13dB. The maximum phase error of ±1.72° is achieved, which is significantly less as compared to the half bit error at the test frequency of 212 MHz.

Acknowledgement

The work was supported by Society for Applied Microwave Electronics Engineering and Research (SAMEER), Department of Electronics and Information Technology (DEITy) Powai, Mumbai. The authors would like to thank Mr. S. S. Kakatkar and Mr. Prathamesh Pednekar affiliated with SAMEER, Mumbai for their valuable comments and support throughout the test of this project.

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